1. An adder circuit for adding a first binary number and a second binary number, the adder comprising:

a carry evaluating circuit generating a carry production control signal representing a sum of a block of corresponding bits of the first binary number and the second binary number and an input carry value to the block, the carry production control signal comprising two signals A and B that can each have a value of either P or Q; and

a conversion circuit coupled to receive the A and B outputs and the conversion circuit outputting two signals X and Y, each having a value of either P or Q, and X and Y having one of three possible values.

2. An adder as in claim 1 wherein X and Y have one of three possible values in accordance with:

	X	Y
Value 1	P	P
Value 2	Q	P
Value 3	Q	Q.

3. An adder as in claim 1 wherein X and Y have one of three possible values in accordance with:

	X	Y
Value 1	P	P
Value 2	P	Q
Value 3	Q	Q.

4. An adder as in claim 1 wherein P=0 and Q=1.

5. An adder as in claim 1 further comprising:

a second circuit coupled to receive the X and Y outputs and outputting a first result if the input carry has a value of 1 and a second result if the input carry has a value of 0.

6. An adder circuit as in claim 1 wherein the carry evaluating circuit is coupled to two pairs of input signals (A_1, b_1) and (A_2, b_2) that comprise one of two respective pairs of bits of the first binary number and the second binary number and two previously evaluated carry production signals.

7. An adder circuit as in claim 1 wherein the carry evaluating circuit is coupled to three pairs of input signals (A_1, b_1), (A_2, b_2) and (A_3, b_3) that comprise one of three respective pairs of bits of the first binary number and the second binary number and three previously evaluated carry production signals.

8. An adder circuit as in claim 1 wherein the carry evaluating circuit is coupled to four pairs of input signals (A_1, b_1), (A_2, b_2), (A_3, b_3) and (A_4, b_4) that comprise one of four respective pairs of bits of the first

binary number and the second binary number and four previously evaluated carry production signals.

9. An adder circuit as in claim 1 wherein the carry evaluating circuit is coupled to N pairs of input signals (A_1, b_1), (A_2, b_2), (A_3, b_3), (A_4, b_4) and (A_n, b_n) that comprise one of N respective pairs of bits of the first binary number and the second binary number and N previously evaluated carry production signals.

10. An adder circuit as in claim 1 wherein a plurality of carry evaluating circuits are used in a parallel prefix structure to evaluate a full set of carry bits from the first binary number and the second binary number.

11. An adder as in claim 1, wherein the carry evaluating circuit is formed of a plurality of static CMOS logic gates.

12. An adder as in claim 1, wherein the carry evaluating circuit is formed of a plurality of dynamic CMOS logic gates.

13. An adder as in claim 1, further comprising:

a carry binary number determining circuit, responsive to the first binary number and the second binary number and generating a carry binary number composed of carry bits of a sum of the first binary number and the second binary number, the carry binary number determining circuit having a plurality of circuit stages operating in series to generate the carry binary number, each circuit stage serving to partially resolve the carry binary number and at least one circuit stage including at least one of the carry bit evaluating circuits generating a carry control production signal that is coupled between the circuit stages as an input signal to a next circuit stage; and

a combinatorial logic circuit coupled to respective corresponding bits of the first binary number, the second binary number and the carry binary number to generate a corresponding bit of a result binary number.

14. An adder as in claim 13, wherein the first, second and carry binary numbers have corresponding bits B1, B2, and B3 respectively, the combinatorial logic circuit performs a logical XOR operation on the three bits.

15. An adder as in claim 1, wherein the carry evaluating circuit is coupled to a microprocessor.

16. An adder as in claim 5, wherein the carry evaluating circuit is coupled to a carry-select circuit.

17. A microprocessor comprising:

an arithmetic logic circuit including an adder having a carry evaluating circuit generating a carry production control signal representing a sum of a block of corresponding bits of the first binary number and the second binary number and an input carry value to the block, the carry production control signal comprising two signals A and B that can each have a value of either P or Q; and

a conversion circuit coupled to receive the A and B outputs and the conversion circuit outputting two signals X and Y, each having a value of either P or Q, and X and Y having one of three possible values.

18. A microprocessor as in claim 17 further comprising:

a second circuit coupled to receive the X and Y outputs and outputting a first result if the input carry has a value of 1 and a second result if the input carry has a value of 0.

19. A microprocessor circuit as in claim 17 wherein the carry evaluating circuit is coupled to two pairs of input signals (A_1, b_1) and (A_2, b_2) that comprise one of two

respective pairs of bits of the first binary number and the second binary number and two previously evaluated carry production signals.

20. A microprocessor circuit as in claim 17 wherein the carry evaluating circuit is coupled to three pairs of input signals (A_1, b_1), (A_2, b_2) and (A_3, b_3) that comprise one of three respective pairs of bits of the first binary number and the second binary number and three previously evaluated carry production signals.

21. A microprocessor circuit as in claim 17 wherein the carry evaluating circuit is coupled to N pairs of input signals (A_1, b_1), (A_2, b_2), (A_3, b_3), (A_4, b_4) and (A_n, b_n) that comprise one of N respective pairs of bits of the first binary number and the second binary number and N previously evaluated carry production signals.

22. A microprocessor circuit as in claim 17 wherein a plurality of carry evaluating circuits are used in a parallel prefix structure to evaluate a full set of carry bits from the first binary number and the second binary number.

23. A microprocessor as in claim 17, further comprising:

a carry binary number determining circuit, responsive to the first binary number and the second binary number and generating a carry binary number composed of carry bits of a sum of the first binary number and the second binary number, the carry binary number determining circuit having a plurality of circuit stages operating in series to generate the carry binary number, each circuit stage serving to partially resolve the carry binary number and at least one circuit stage including at least one of the carry bit evaluating circuits generating a carry control production signal that is passed between the circuit stages as an input signal to a next circuit stage; and

a combinatorial logic circuit responsive to respective corresponding bits of the first binary number, the second binary number and the carry binary number to generate a corresponding bit of a result binary number.

24. A microprocessor as in claim 23, wherein the first, second and carry binary numbers have corresponding bits B1, B2, and B3 respectively, the combinatorial logic circuit performs a logical XOR operation on the three bits.

25. A microprocessor as in claim 23, wherein the carry evaluating circuit is coupled to a carry-select circuit.

26. A method for adding a first and a second binary number, each having a plurality of bits, comprising:

generating a carry production control signal representing a sum of a plurality of corresponding bits of the first binary number and the second binary number and an input carry value to the plurality of bits where the carry production control signal comprises two signals A and B that can each have a value of either P or Q; and

converting the A and B signals into two signals, X and Y, representing one of three possible values.

27. The method of claim 26 further comprising:

receiving the X and Y signals and generating a first result if the input carry has a value of 1 and a second result if the input carry has a value of 0.

28. The method of claim 27 further comprising:

receiving the X and Y signals and generating a final result utilizing a carry-select evaluator circuit.

29. The method of claim 27 further comprising:

determining a final binary result of adding the first and second binary numbers by utilizing a plurality of carry evaluating circuits in a parallel prefix structure to generate a full set of carry bits from the first binary number and the second binary number.